

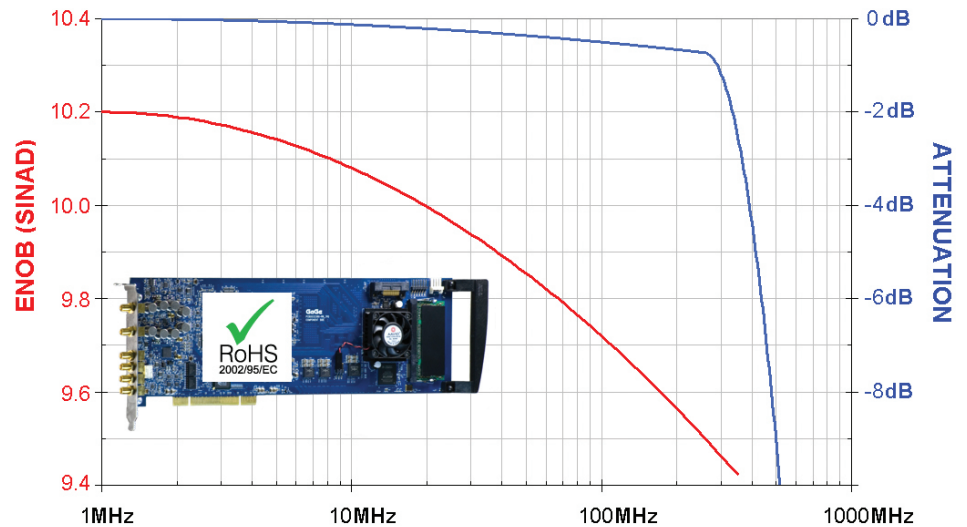
The 12-bit CompuScope 12501 and 12502 provide the highest available Effective Number of Bits (ENOB (SINAD)) performance at high signal frequency that is available on the market.

## APPLICATIONS

Radar Design and Test  
 Disk Drive Testing  
 Manufacturing Test  
 Signal Intelligence  
 Lidar Systems  
 Communications  
 Non-Destructive Testing  
 Spectroscopy  
 High-Performance Imaging  
 Ultrasound Test

## CompuScope 12501/12502

### 12-Bit Ultra-high Performance Digitizers for the PCI Bus



CS12501 and CS12502 attain a new level of signal fidelity in high-speed digitizer performance.

## FEATURES

- 1 or 2 digitizing channels
- 500 MS/s maximum sampling per channel
- 12 bits vertical resolution
- 128 MS to 2 GS on-board acquisition memory
- 350 MHz bandwidth
- Frequency Response Flat with  $\pm 1$  dB in first Nyquist zone
- Extremely high Effective Number of Bits  
 ENOB (SINAD) = 10.1 at 10 MHz  
 ENOB (SINAD) = 9.5 at 200 MHz
- Full-featured front-end, with software control over input ranges, coupling and filters
- Synchronize up to 8 cards in a Master/Slave mode
- Low power consumption (15 Watts typical)
- 32 bits, 66 MHz PCI standard for 200 MB/s transfer to PC memory
- Ease of integration with External and Reference Clock In and Clock Out, External Trigger In and Trigger Out
- Programming-free operation with GageScope® oscilloscope software
- Software Development Kits available for LabVIEW, MATLAB and C/C#

## **MAIN CS12501/CS12502 SPECIFICATIONS**

<b>Model</b>	<b>Number of Input Channels</b>	<b>Maximum Sampling Rate</b>	<b>Input Bandwidth (-3 dB Point)</b>
<b>CS12501</b>	1	500 MS/s	350 MHz
<b>CS12502</b>	2	500 MS/s	350 MHz

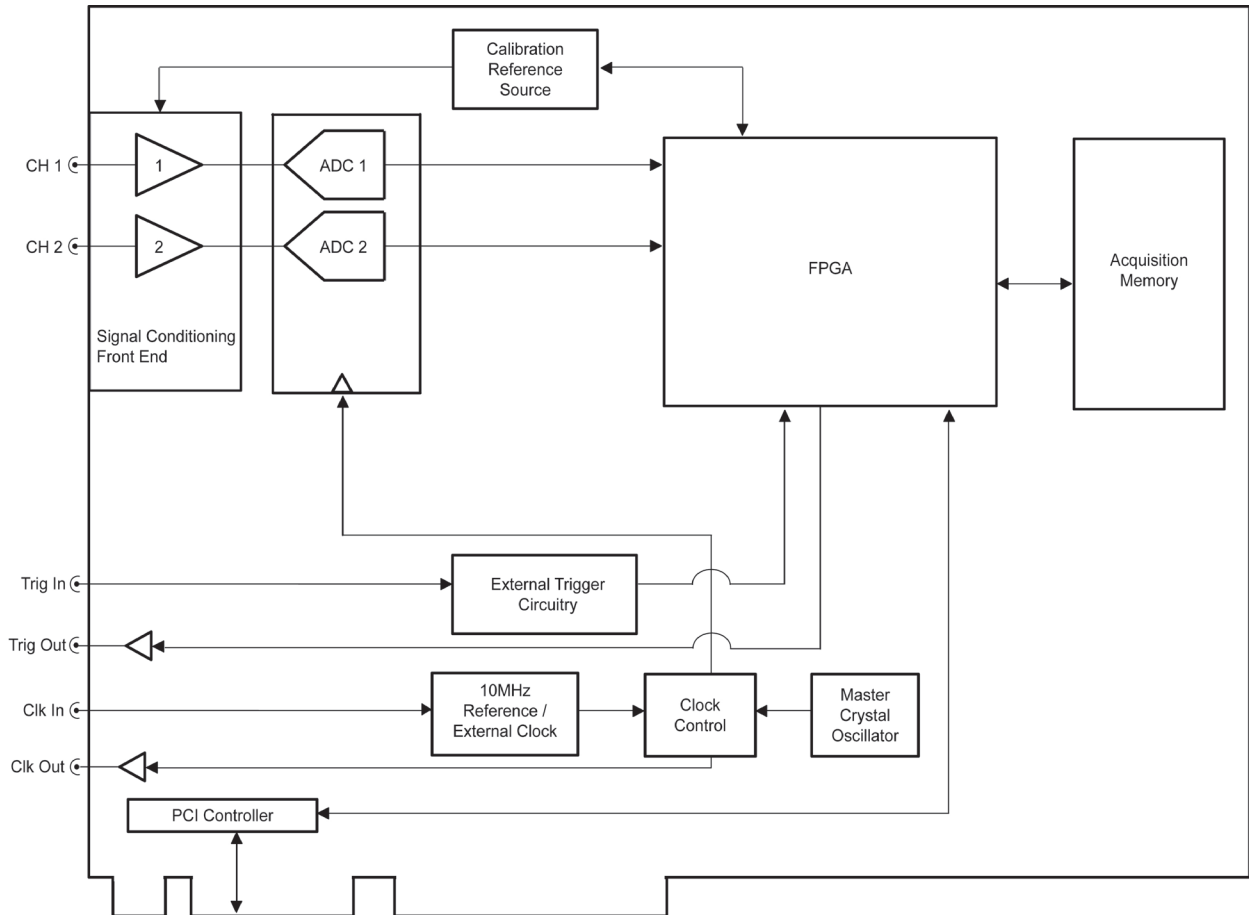
Vertical Resolution: 12-bits  
Basic Acquisition Memory<sup>1</sup>: 128 MegaSamples  
Available Acquisition Memory Options: 256 MS, 512 MS, 1 GS, 2 GS

### **CHANNEL SPECIFICATIONS**

Channel Input Voltage Ranges:  $\pm 100$  mV,  $\pm 200$  mV,  $\pm 500$  mV,  $\pm 1$  V,  $\pm 2$  V,  $\pm 5$  V (software-selectable)  
Channel Impedance:  $50 \Omega \pm 2\%$   
Channel Coupling: AC or DC (software-selectable)  
Channel DC User Offset<sup>2</sup>: Spans Full Scale Input Range (FSIR) (software-selectable)  
Channel Low-Pass Filter: 5-Pole with -3dB point at 70 MHz  
(May be independently software-selected for each input channel)  
Channel-to-Channel Isolation: Better than -95 dB  
Channel Absolute Max Input<sup>3</sup>:  $\pm 10$  V

1 Memory is divided among the all active channels (1 or 2)  
2 Adjustable in 1/2 % steps. On  $\pm 500$  mV and  $\pm 5$  V range offset is limited to  $\pm 240$  mV and  $\pm 2.4$  V, respectively.  
3 On  $\pm 500$  mV,  $\pm 200$  mV and  $\pm 100$  mV input ranges, input signal is automatically switched away from input circuitry if it exceeds roughly  $\pm 2$  V.

## CompuScope 1250X Simplified Block Diagram



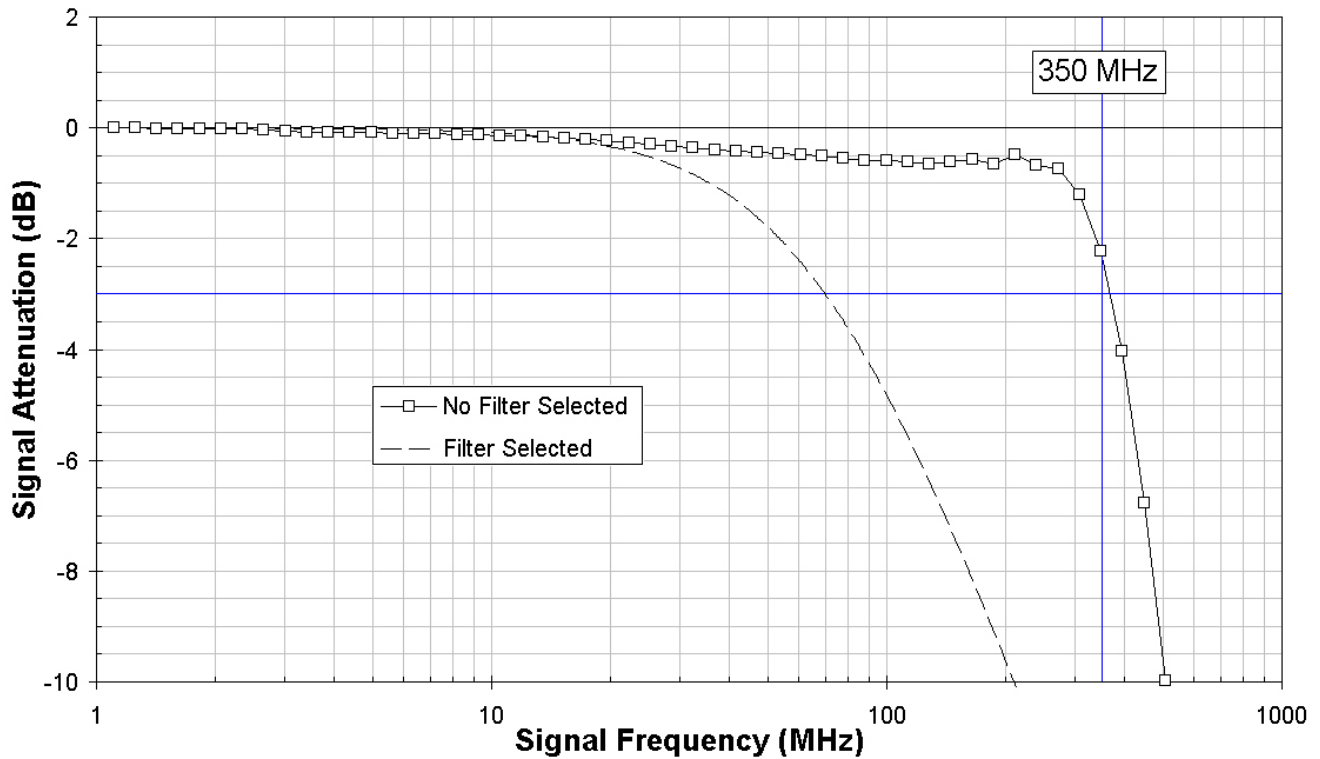
### PHYSICAL/MECHANICAL

Length:	312.00 mm / 12.283"
Width:	< 14.5 mm/0.570" (neighboring PCI slots are accessible)
Height:	106.68 mm / 4.200"
Weight:	< 0.33 Kg / 0.75 lbs
Connectors:	SMA

### PCI INTERFACE

PCI Speed:	32-bit PCI – 33 or 66 MHz
PCI Power:	Universal - 3.3 Volt or 5 Volt

## CHANNEL FREQUENCY RESPONSE



Note: Typical Frequency Response curves above taken on the  $\pm 500$  mV input range with  $50 \Omega$  termination and DC coupling. In AC coupling mode, the lower -3 dB cutoff is at 20 kHz.

Input Range	CS12501/CS12502	
	Bandwidth (MHz)	Flatness (MHz)
$\pm 2$ V	365	310
$\pm 500$ mV	370	290
$\pm 100$ mV	345	285

Note: The *Bandwidth* is defined as frequency at which the signal attenuation falls below -3 dB of its value at a 1 MHz signal frequency. The *Flatness* is the frequency below which the signal attenuation is constant within  $\pm 1$  dB of its value at a 1 MHz signal frequency.

Rise Time<sup>1</sup>: 1.0 nanoseconds (Typical)

<sup>1</sup> The Rise Time is calculated as  $0.35/\text{Bandwidth}$

## **CHANNEL ABSOLUTE ACCURACY**

DC Gain and Offset Error are presented as a function of the Full-Scale Input Range (FSIR). For example, on the  $\pm 1$  Volt Input Range, the FSIR is 2 Volts.

Absolute DC Gain Error (Volts):  $< \pm 0.5\% \times (\text{FSIR})$   
e.g. Gain Error  $< 0.5\% \times 2\text{V} = 10 \text{ mV}$  on  $\pm 1 \text{ V}$  Input Range ( $50\Omega$ )

Absolute DC Offset Error (Volts):  $< \pm (0.1\% \times (\text{FSIR}))$   
e.g.  $< 0.1\% \times 2\text{V} = 2 \text{ mV}$  on  $\pm 1 \text{ V}$  Input Range ( $50\Omega$ )

Notes:

The Maximum Absolute DC Error may be calculated by summing the Absolute DC Gain Error and the Absolute DC Offset Error in quadrature

$$\text{Maximum Absolute DC Error} = \sqrt{(\text{Absolute DC Gain Error})^2 + (\text{Absolute DC Offset Error})^2}$$

For example, on the  $\pm 1$  Input Range

$$\text{Maximum Absolute DC Error} = \sqrt{(0.5\% \times 2\text{V})^2 + (0.1\% \times 2\text{V})^2}$$

Maximum Absolute DC Error  $< 10.2 \text{ mV}$

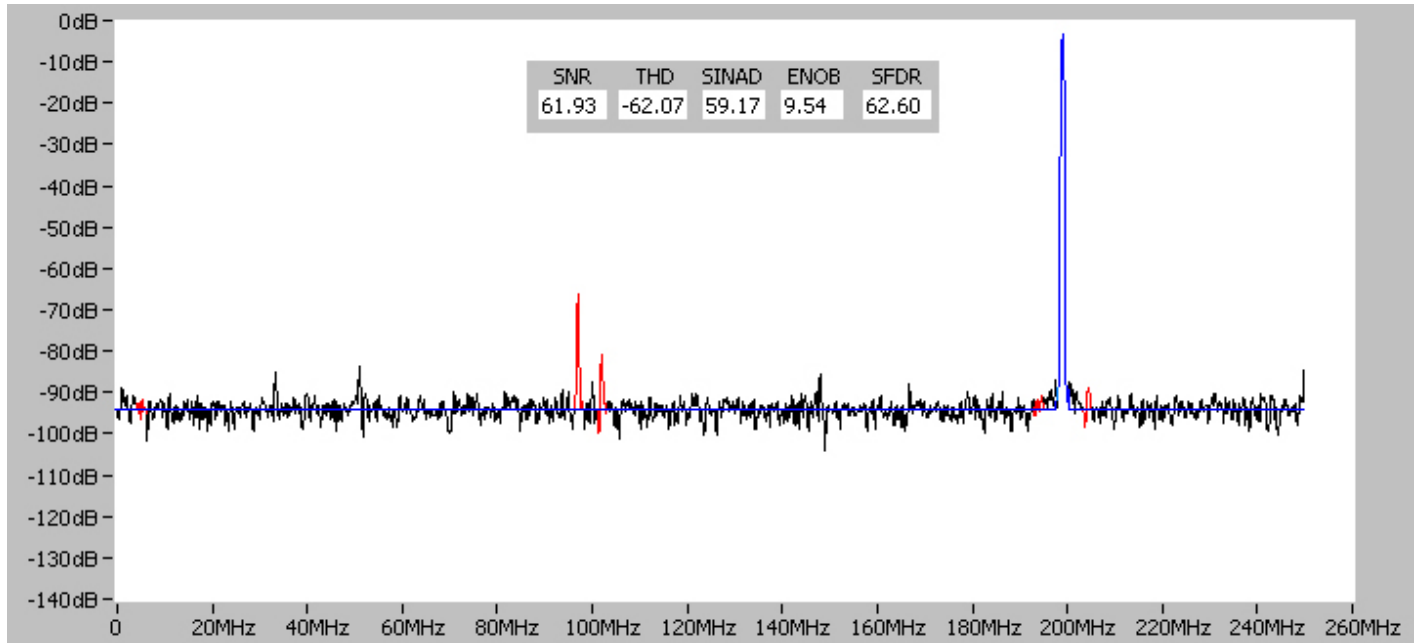
Maximum Absolute DC Error  $< 0.51\%$  of FSIR

These values relate only to the Absolute accuracy of the CompuScope 12501/12502 boards and say nothing about the relative accuracy. Relative accuracy performance is superior and is provided by the Dynamic Performance Parameters.

Each time that a new input configuration (e.g. Input range, termination, coupling) is selected, the CS12501/12502 undergo an on-board auto-calibration sequence, which corrects for component value changes due to aging or thermal drift.

Before shipment, all CompuScope 12501/12502 boards are tested at the factory using the Gage Performance Verification System. This system introduces DC voltages from a NIST-traceable calibrator source to the card in all input configurations and confirms that no measured errors are worse than the errors listed above.

## DYNAMIC PERFORMANCE



Frequency spectrum above taken on a CS12501 on its  $\pm 500$  mV input range with DC coupling.

Dynamic Parameters are measured by acquiring a high-purity 199 MHz sine wave signal, deriving an associated Fourier Spectrum and identifying the Fundamental Power (F), the Noise Power (N) and the Harmonic Power (H). These Powers are measured as the areas under the frequency bins respectively indicated in blue, red and black in the frequency spectrum above.

### **DYNAMIC PARAMETERS DEFINITIONS**

Signal-to-Noise Ratio (SNR)  $\equiv 10 \times \log (F/N)$

Total Harmonic Distortion (THD)  $\equiv 10 \times \log (H/F)$

Signal-to-Noise-and-Distortion Ratio (SINAD)  $\equiv 10 \times \log (F/(H+N))$

Effective Number Of Bits (ENOB)  $\equiv (SINAD - 1.76 \text{ dB})/6.02 \text{ dB}$

Spurious Free Dynamic Range (SFDR)  $\equiv$  Amplitude of highest spurious spectral peak

RMS Noise  $\equiv$  Standard Deviation of acquired signal with CompuScope input loaded with external  $50\Omega$  terminator.

Dynamic Parameters with 10 MHz Signal Frequency <sup>1</sup>					
Input Range	SNR	THD	SINAD	ENOB	SFDR
±500 mV	62.2 dB	-75.0 dB	62.0 dB	10.0	81.0 dB
±100 mV	56.2 dB	-71.0 dB	56.0 dB	9.0	78.6 dB
Dynamic Parameters with 70 MHz Signal Frequency <sup>1</sup>					
Input Range	SNR	THD	SINAD	ENOB	SFDR
±500 mV	61.7 dB	-68.9 dB	61.0 dB	9.8	64.9 dB
±100 mV	56.0 dB	-68.5 dB	55.8 dB	9.0	75.2 dB
Dynamic Parameters with 199 MHz Signal Frequency <sup>1</sup>					
Input Range	SNR	THD	SINAD	ENOB	SFDR
±500 mV	61.0 dB	-61.7 dB	58.3 dB	9.4	62.0 dB
±100 mV	56.1 dB	-65.7 dB	55.7 dB	9.0	68.9 dB

RMS Noise on Select Input Ranges				
Input Range	±100 mV	±500 mV	±2 V	±5V
<b>CS1250X</b>	100 $\mu$ V	250 $\mu$ V	1.2 mV	2.5 mV

<sup>1</sup> All data acquired with DC coupling and with no low-pass filters activated.

## **TIME-DOMAIN SAMPLING**

Internal Sampling Rates: 500 MS/s, 250 MS/s, 125 MS/s, 50 MS/s, 25 MS/s, 10 MS/s, 5 MS/s, 2.5 MS/s, 1MS/s  
1 MS/s, 500 kS/s, 250 kS/s, 100 kS/s, 50 kS/s, 25 kS/s, 10 kS/s

Internal Sampling Rate Accuracy/Stability<sup>1</sup>: 1 part-per-million  
Channel-to-Channel Skew<sup>2</sup>: Less than 300 picoseconds

### **CLOCK IN**

Clock In Signal Level: Minimum 300 mV peak-to-peak  
Maximum 5 V peak-to-peak

Clock In Signal Input Termination: 50  $\Omega$   
Clock In Signal Input Coupling: AC  
Clock In Signal Duty Cycle: 50%  $\pm$  5%

Clock In Modes:

1. External Clock – Input signal is used as a sampling clock signal and directly clocks ADC chips
2. 10 MHz Reference – High accuracy 10 MHz input signal disciplines the internal sampling oscillator so that, for example, a 500 MS/s sampling rate is at exactly 50X the 10 MHz reference frequency

Maximum External Clock Frequency: 500 MHz  
Minimum External Clock Frequency: 160 MHz  
10 MHz Reference Mode Frequency: 10 MHz  $\pm$  1 kHz

### **CLOCK OUT**

Clock Out Mode: 10 MHz Reference Clock Out  
Clock Out Signal Level:  $\pm$ 1 V into 50  $\Omega$   
 $\pm$ 2 V into 1 M $\Omega$

Clock Out Signal Output Termination: 50  $\Omega$

Clock Out Coupling: AC

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1 Master Sampling Oscillator is disciplined by an on-board temperature-compensated 10 MHz reference signal with 1 part-per-million accuracy and stability.

2 Channels use same input settings

## **TRIGGERING**

Trigger Source:	Any Input Channel, External Trigger or Software
Trigger Level:	Software controllable analog Trigger level with span of the Full Scale Input Range (FSIR) of the Trigger Source. Adjustable in ½ % steps
Trigger Slope:	Positive or Negative (software-selectable)
Trigger Engines:	2 per Input Channel, 1 for External Trigger - results logically ORed to create trigger event
Trigger Jitter <sup>1</sup> :	1 Sample
Trigger Hold-off:	Allows triggers to be ignored in order to ensure acquisition of any pre-set amount of pre-trigger data.
Trigger Delay:	Allows suppression of the acquisition of any amount of post-trigger data in order to conserve memory for the acquisition of only later waveform data.

## **INTERNAL TRIGGERING**

Internal Trigger Sensitivity <sup>2</sup> :	±2% of Full Scale Input Range of Trigger Source
Internal Trigger Level Accuracy:	Better than ±2% of Full Scale

## **EXTERNAL TRIGGERING**

External Trigger Input Voltage Ranges:	±1 V, ±5 V (software-selectable)
External Trigger Coupling:	AC or DC (software-selectable)
External Trigger Input Impedance:	1 kΩ or 50 Ω (software-selectable)
External Trigger Input Bandwidth:	>150 MHz
External Trigger Absolute Max Input:	±6 V
External Trigger Sensitivity:	±5% of Full Scale External Trigger Range
External Trigger Level Accuracy:	±10% of Full Scale External Trigger Range

## **TRIGGER OUT<sup>3</sup>**

Trigger Out Signal Level:	0 - 2 V into 50 Ω 0 - 1 V into 1 MΩ
Trigger Out Signal Output Termination:	50 Ω compatible

1 This jitter applies for an asynchronous trigger and sampling clock. Sub-nanosecond jitter may be achieved using synchronous trigger and sampling clock

2 Signal amplitude must be at least 4% of Full Scale Input Range of Trigger Source to cause a trigger event. Smaller signals are rejected as noise.

3 The Trigger Out signal is useful for triggering user signals so that they are synchronous with the CompuScope's internal sampling clock

## **GENERAL COMPUSCOPE ACQUISITION**

### **ACQUISITION MODES:**

1. Single Record Mode – In Single Record Mode, each waveform is downloaded to PC RAM, where it is accessible to the user, prior to the next waveform acquisition.
2. Multiple Record Mode – In Multiple Record Mode, acquired waveforms are stacked in on-board Compuscope memory for later download. Between successively triggers, the acquisition circuitry is rapidly re-armed in hardware with no software communication required.

Segment Memory is the amount of memory available to hold waveform data, which may include both pre- and post-trigger data

Post-Trigger Data: 32 Sample minimum up to full Segment Memory. Post-trigger Depth may be increased in steps of 32 Samples.

Pre-Trigger Data: Up to full Segment Memory (**Single Record Mode**)

Up to 128 kiloSamples (**Multiple Record Mode**)

### **MAXIMUM SEGMENT MEMORY**

Single Record Mode<sup>1, 2</sup>:

Max Segment Memory  $\approx$  Total on-board memory / Number of Active Channels

Multiple Record Mode<sup>2</sup>:

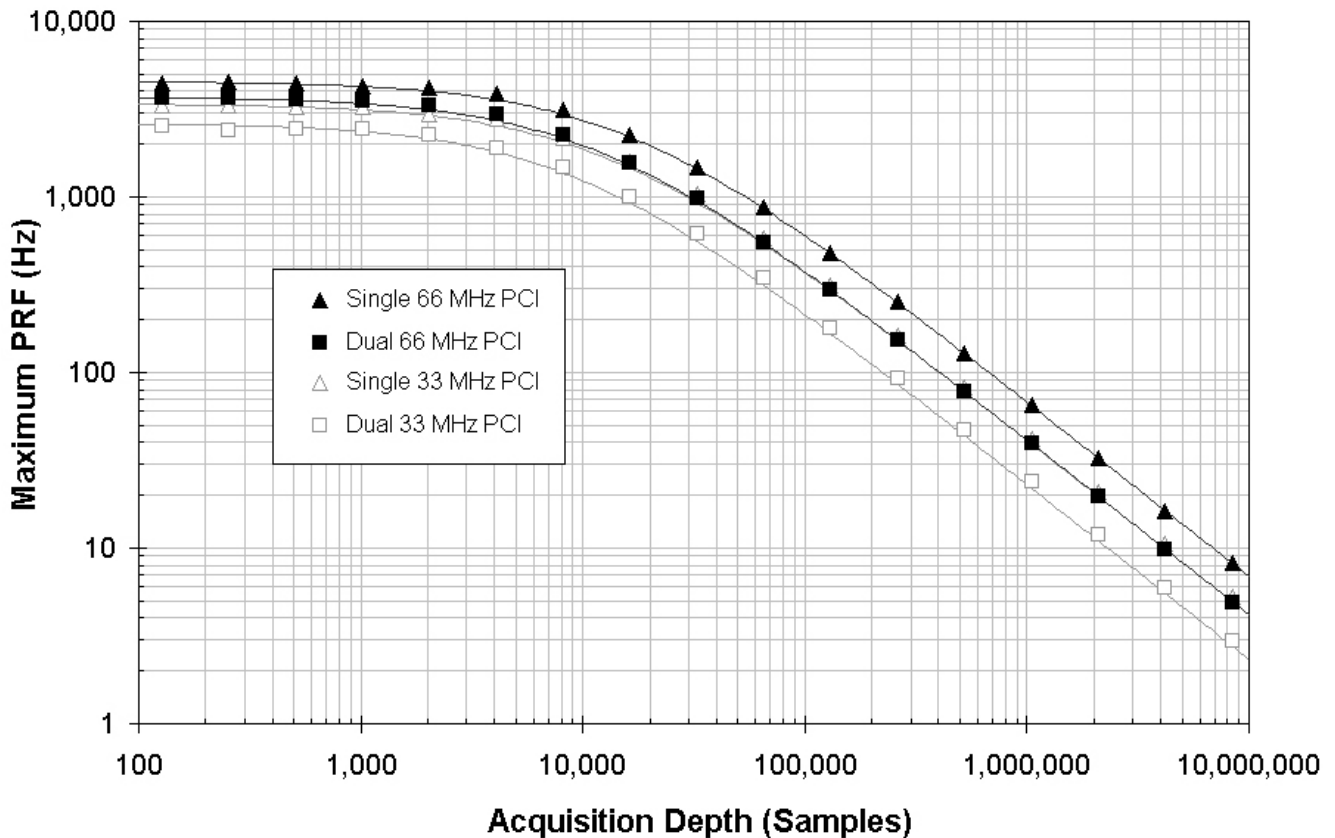
Segment Memory  $\approx$  Total on-board memory / Number of Active Channels / Number of Segments

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1 Number of Active Channels may be 1 or 2.

2 The above equation is not exact due to storage of a small amount of inter-record data, such as Time-Stamping Information.

## SINGLE RECORD MODE ACQUISITION



### Repetitive Waveform Acquisition Performance

The plot above shows the CS12501/12502's maximum Pulse Repeat Frequency (PRF), which is the maximum trigger rate without trigger loss. Curves are shown with a sampling rate of 500 MS/s for acquisition of 1 and 2 channels (Single and Dual) and for PCI clock speeds of 33 MHz and 66 MHz. (In practice, 66 MHz PCI usually implies PCI-X). Straight line portions of the curves at high Depths provide measurement of PCI bus-mastering transfer speeds of over 100 Megabytes/second and 200 Megabytes/second respectively for 33 MHz and 66 MHz PCI.

No data processing or storage to hard drive were performed for the PRF measurements and performance may vary slightly with system configuration.

## MULTIPLE RECORD MODE ACQUISITION

Multiple Record Inter-Trigger Re-arm time: Less than 4 microseconds

Note: Because the no software communication is required during a Multiple Record acquisition, the Re-arm time is completely deterministic or invariant. For example, an acquisition of duration 6 microseconds could be triggered at a rate of up to  $1/(6 \mu\text{s} + 4 \mu\text{s}) = 100 \text{ kHz}$  with a guarantee of no loss of triggers.

## TRIGGER TIME-STAMPING

The Trigger Time –Stamping functionality tags the occurrence time of trigger events using a wide high–speed on-board counter that has high accuracy and is independent of any Host PC timing.

Time–Stamping Counter Clock source:	Fixed 137.5 MHz on-board oscillator or one-fourth of Sampling Clock (software-selectable)
Time–Stamping Counter Resolution:	One clock cycle
Time–Stamping Counter Width:	44-bits
Time–Stamping Counter Rollover time <sup>1</sup> :	39 hours or more

## MULTI-COMPUSCOPE SYSTEMS

### Master/Slave CompuScope Mode

Number of Master/Slave CS1250X CompuScopes:	2-8 cards
Board-to-Board Timing Skew:	TBA

Note: In a Independent CompuScope system, identical CompuScopes are configured to behave from a hardware and software perspective as a single multi-channel digitizer system. All CompuScopes within a Master/Slave system will sample, trigger and re-arm simultaneously. CompuScopes self-configure as a Master/Slave system upon detection of the internal Master/Slave inter-CompuScope bridge-board connector. This system may be broken up into independent CompuScopes simply by not installing the bridge-board.

### Independent CompuScope Mode

Number of Master/Slave CS1250X CompuScopes: Number limited only by number of PCI slots in backplane and available DC power.

Note: Users may install independent CompuScopes, which may be different models, within a single host PC. Independent CompuScopes may trigger and sample asynchronously. Independent asynchronous Compuscope operation is fully supported by GageScope and all Compuscope Software Development Kits (SDKs).

## POWER CONSUMPTION

PCI DC SUPPLY	CS12501	CS12502
+5 V	5.8 W	7.2 W
+3.3 V	5.3 W	6.2 W
+12 V	1.3 W	2.6 W
-12 V	0.3 W	0.4 W
-5 V	0	0
<b>Total</b>	< 13 W	< 17 W

Note: The consumption values above are for CS12501/12502 CompuScopes with the base acquisition memory of 128 MegaSamples. For a 2 GigaSample Compuscope, the extra power consumption is 3 Watts. For intermediate memory options, the extra consumption increases in proportion to the amount of memory.

<sup>1</sup> At the top Time-Stamping Counter clocking rate of 500 MHz/4, the counter rollover time is  $2^{44}/125 \text{ MHz} > 39$  hours

## **CS12501/12502 – AUXILIARY INPUT/OUTPUT OPTION**

With this option, the CS1250X is equipped with two additional SMA connectors on its back-plate – a Digital Input connector and a Digital Output connector. The functionality of these connections may be software-selected as one of the functionalities listed below. Call factory for custom Digital Input/Output requirements.

### **DIGITAL INPUT**

Signal Level: 0-5 V TTL

#### Digital Input Functionalities

**Trigger Enable:** After acquisition begins, trigger events are ignored until a rising (or falling) edge on the Digital Input signal is detected. The Trigger Enable input can also be configured in Gate Mode, where triggers are accepted or ignore based on the signal level. The functionality is useful for Video signal frame applications or in hard drive testing.

**Time-Stamp Reset:** Upon detection of a rising edge on the digital Input sign, the CompuScope resets the value of the Time Stamping counter to 0. This feature is useful to synchronize the CompuScope Time-Stamping counter to external timing reference events from, for example, an IRIG device.

### **DIGITAL OUTPUT**

Signal Level: 0-5 V TTL

#### Digital Output Functionalities

**Busy Out:** This Digital Output signal goes HIGH while the CompuScope is acquiring waveform data and remains LOW otherwise. It is useful to synchronize other devices with the beginning or end of CompuScope acquisition. One important example is the triggering of a second CompuScope by the falling edge Busy Out so that acquisition is continued on this second CompuScope.



## HOST PC SYSTEM REQUIREMENTS

PCI-based computer, minimum Pentium IV 1.5 GHz, with at least one free full-length PCI slot, 256 MB RAM, 150 MB hard disk.

### Operating System:

Windows 7:	All Versions (32/64-bit)
Windows Vista:	All Versions (32/64-bit)
Windows XP:	All Versions (32/64-bit)
Windows Server:	2003, 2008
Linux Version:	Debian 5

## SOFTWARE SUPPORT

### Application Software:

GageScope is a Windows-based software for programming-free CompuScope operation

GageScope LITE Edition: Included with purchase, provides basic functionality

GageScope Standard Edition: Provides limited functionality of advanced analysis tools, except for Extended Math

GageScope Professional Edition: Provides full functionality of all advanced analysis tools

### Software Development Kits:

CompuScope SDK for C/C# for Windows

Includes: CompuScope C SDK for Windows<sup>1</sup>

CompuScope .NET SDK for Windows<sup>2</sup>

CompuScope SDK for MATLAB for Windows

CompuScope SDK for LabVIEW for Windows

## FIRMWARE SUPPORT

eXpert Signal Averaging Firmware Option

Call factory for custom eXpert Signal Processing Firmware

## OPERATING TEMPERATURE

Internal PC Temperature Range: 0 °C to +65 °C

## CERTIFICATION

CE: Pending

FCC: Pending

RoHs: Compliant

<sup>1</sup> C SDK is compatible with LabWindows/CVI 7.0 +

<sup>2</sup> .NET SDK is CLR compliant and includes support for Visual Basic.NET and Delphi



**WARRANTY**

One year parts and labor  
Certificate of NIST Traceable Calibration is included.

\*All specifications subject to change without notice.

**ORDERING INFORMATION**

**Hardware & Upgrades**

CS12501 (1 channel, 12-bit, 500 MS/s) 120-501-001  
CS12502 (2 channels, 12-bit, 500 MS/s) 120-502-001

Memory Upgrade: 128 MS to 256 MS 120-181-001  
Memory Upgrade: 128 MS to 512 MS 120-181-003  
Memory Upgrade: 128 MS to 1 GS 120-181-005  
Memory Upgrade: 128 MS to 2 GS 120-181-007

Set 1 Cable SMA to BNC ACC-001-031  
Set 4 Cable SMA to BNC ACC-001-033

CS12501: Auxiliary Input/Output Option 120-181-101  
CS12502: Auxiliary Input/Output Option 120-181-102

Master Multi-Card Upgrade 120-181-002  
Slave Multi-Card Upgrade 120-181-003

eXpert™ Firmware Options  
eXpert Signal Averaging Firmware Option 250-181-001

**GageScope® Software**

GageScope: Lite Edition Included  
GageScope: Standard Edition 300-100-351  
(with Purchase of CompuScope Hardware)  
GageScope: Professional Edition 300-100-354  
(with Purchase of CompuScope Hardware)

**Software Development Kits (SDKs)**

GaGe SDK Pack on CD 200-113-000  
CompuScope SDK for C/C# 200-200-101  
CompuScope SDK for MATLAB 200-200-102  
CompuScope SDK for LabVIEW 200-200-103

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Updated Mar 1, 2011

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